4462

Reg. No. : ....

Name : ....

Fourth Semester B.Tech. Degree Examination, July 2015
(2008 Scheme)
08.403 : COMPUTER HARDWARE DESIGN (R)

Time : 3 Hours

Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4 marks each**.

1. Write the algorithm and draw the hardware for signed 2's complement addition and subtraction.

2. What is an array multiplier ? Show the implementation of a 2×2 array multiplier.

3. Differentiate fixed point and floating point binary data representation.

4. Design a 4 bit combinational logic shifter.

5. Design an arithmetic circuit with one selection variable S and two data inputs A and B. When S = 0, the circuit performs the addition operation F = A + B. When S = 1, the circuit performs the increment operation F = A + 1.

6. What is a scratchpad memory ? What is its use ?

7. Why control logic design is done using specialized methods rather than sequential logic procedure ?

8. Explain the one flip flop per state method of control organization.

9. What is PLA ?

10. What is the use of a micro program sequencer ?

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PART – B

Answer **any one** full question from **each** Module. **Each** full question carries **20** marks.

Module – I

11. Write the algorithm and draw the hardware for booth multiplication algorithm of signed 2's complement representation. Illustrate the method.   **20**

OR

12. Explain restoring and non restoring methods of binary division with example.   **20**

Module – II

13. a) Which are the different types of micro operations used in register transfer language ? Explain each category.   **10**

b) Show the hardware that implements the following statement. Include the logic gates for the control function.   **10**

$$xy'T_0 + T_1 + x'yT_2 : A \leftarrow A + B$$

OR

14. a) Design a 4 bit status register for an 8 bit ALU. The status bits represents carry, sign, zero and overflow.   **10**

b) Which are the alternatives for organizing a general purpose processor unit ? How they differ from one another ?   **10**

Module – III

15. Draw the block diagram of micro program sequencer and explain its operations. How it is used in computer CPU ?   **20**

OR

16. Design a hardwired control for multiplication of two fixed point binary numbers in sign magnitude representation.   **20**